



PATENTS
ALT-155

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Applicants : Tony K. Ngai et al.
Application No.: 09/124,649
Filed : July 29, 1998
For : PROGRAMMABLE LOGIC DEVICE HAVING
EMBEDDED DUAL-PORT RANDOM ACCESS MEMORY
CONFIGURABLE AS SINGLE-PORT MEMORY
Group Art Unit : 2752
Examiner : Pierre-Michel Bataille

New York, New York 10020
October 20, 2000

Hon. Commissioner for Patents
Washington, D.C. 20231

SECOND SUPPLEMENTAL
INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §§ 1.56 and 1.97, applicants hereby make the following patents and publications of record in the above-identified patent application:

Kaplinsky U.S. Patent No. Re 34,444 (November 16, 1993)
Patil U.S. Patent No. 4,293,783 (October 6, 1981)
Carter U.S. Patent No. 4,642,487 (February 10, 1987)
Carter U.S. Patent No. 4,706,216 (November 10, 1987)
Carter U.S. Patent No. 4,758,985 (July 19, 1988)
Kawata U.S. Patent No. 4,825,414 (April 25, 1989)
Imazeki et al. U.S. Patent No. 4,831,591 (May 16, 1989)
Ikeda U.S. Patent No. 4,855,958 (August 8, 1989)
Freeman U.S. Patent No. 4,870,302 (September 26, 1989)
Nakayama et al. U.S. Patent No. 4,903,236 (February 20, 1990)
Keida U.S. Patent No. 4,963,770 (October 16, 1990)

Steele U.S. Patent No. 4,975,601 (December 4, 1990)
 Agrawal et al U.S. Patent No. 5,042,004 (August 20, 1991)
 Neal et al. U.S. Patent No. 5,089,993 (February 18, 1992)
 Steele U.S. Patent No. 5,099,150 (March 24, 1992)
 Chan et al. U.S. Patent No. 5,122,685 (June 16, 1992)
 Steele U.S. Patent No. 5,128,559 (July 7, 1992)
 Oh U.S. Patent No. 5,138,577 (August 11, 1992)
 Steele U.S. Patent No. 5,144,582 (September 1, 1992)
 Agrawal et al. U.S. Patent No. 5,212,652 (May 18, 1993)
 Cliff et al. U.S. Patent No. 5,258,668 (November 2, 1993)
 Pedersen et al. U.S. Patent No. 5,260,610 (November 9, 1993)
 Cliff et al. U.S. Patent No. 5,260,611 (November 9, 1993)
 Scott et al. U.S. Patent No. 5,291,444 (March 1, 1994)
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 Agrawal et al. U.S. Patent No. 5,329,460 (July 12, 1994)
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 Freeman et al. U.S. Patent No. 5,343,406 (August 30, 1994)
 New U.S. Patent No. 5,349,250 (September 20, 1994)
 Watson U.S. Patent No. 5,352,940 (October 4, 1994)
 Stansfield U.S. Patent No. 5,408,434, (April 18, 1995)
 Freidin U.S. Patent No. 5,414,377 (May 9, 1995)
 Liu et al. U.S. Patent No. 5,425,036 (June 13, 1995)
 Ong U.S. Patent No. 5,426,378 (June 20, 1995)
 Pedersen et al. U.S. Patent No. 5,436,575 (July 25, 1995)
 Huang U.S. Patent No. 5,448,522 (September 5, 1995)
 Yumitori et al. U.S. Patent No. 5,471,425 (November 28, 1995)
 Cliff et al. U.S. Patent No. 5,550,782 (August 27, 1996)
 Freidin et al. U.S. Patent No. 5,566,123 (October 15, 1996)
 Steele et al. U.S. Patent No. 5,809,281 (September 15, 1998)
 Tsui et al. U.S. Patent No. 5,835,405 (November 10, 1998)
 European Pat. Off. 0 081 917 (June 22, 1983)
 European Pat. Off. 0 420 389 (April 3, 1991)

European Pat. Off. 0 415 542 (March 6, 1991)
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European Pat. Off. 0 507 507 (October 7, 1992)
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Electronic Engineering, 64, No. 786, June 1992, pp. 9-10

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pp. 1-87 (Advance Data Sheet, Feb. 1985)

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Bursky, D., "Denser, Faster FPGAs Vie for Gate-Array
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1993, pp. 55-75

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1992, pp. 35-43

Bursky, D., "Shrink Systems with One-Chip Decoder,
EPROM, and RAM," Electronic Design, July 28, 1988, pp. 91-94

Casselman, "Virtual Computing and The Virtual
Computer," IEEE, July 1993, p. 43

Hsieh et al., "Third Generation Architecture Boosts
Speed and Density of Field Programmable Gate Arrays," Proc.
of IEEE CICC Conf., May 1990, pp. 31.2.1 to 31.2.7

Intel Preliminary Datasheet, "iFX780: 10ns FLEXlogic
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Kautz, "Cellular Logic-in-Memory Arrays," IEEE Trans.
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Interconnect Architecture for User-Reprogrammable Gate
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Ling et al., "WASMII: A Data Driven Computer on a Virtual Hardware," Proc. of IEEE Field Prog. Custom Computing Machines Conf., Napa, California, April 1993, pp. 33-42

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Masumoto, R.T., "Configurable On-Chip RAM Incorporated into High Speed Logic Array," IEEE Custom Integrated Circuits Conference, Jun. 1985, CH2157-6/85/0000-0240, pp. 240-43

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Quenot et al., "A Reconfigurable Compute Engine for Real-Time Vision Automata Prototyping," Proc. of IEEE FCCM Conf., Napa, California, February 1994, pp. 91-100

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Sato, H. et al., "A 209K-Transistor ECL Gate Array with RAM," IEEE Jor. of Solid-State Circuits, Vol. 24, No. 5, October 1989, pp. 1275-79

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Copies of the aforementioned patents and publications, which are listed on the accompanying Form PTO-1449 (submitted in duplicate), are enclosed herewith.

It is respectfully requested that these patents and publications be (1) fully considered by the Patent and Trademark Office during the examination of this application; and (2) printed on any patent which may issue on this application. Applicant requests that a copy of Form PTO-1449, as considered and initialled by the Examiner, be returned with the next communication.

A check in the amount of \$240.00, in payment of the fee set forth in 37 C.F.R. § 1.17(p), is enclosed herewith. The Director is hereby authorized to charge any additional fee that may be due, or credit any overpayment, in connection with this Second Supplemental Information Disclosure Statement, to Deposit Account No. 06-1075. A duplicate copy of this Second Supplemental Information Disclosure Statement is enclosed herewith.

An early and favorable action is respectfully
requested.

Respectfully submitted,



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